AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 6, lines 4-27, with the following amended paragraph:

Returning to FIG. 1, Gray code counter 20 can be implemented in any of a variety of ways (e.g., as a finite state machine outputting the desired Gray code sequence in response to successive WCLK signal cycles). However counter 20 is implemented, the output signals should be free of "glitches" (i.e., momentarily erroneous or indefinite states). FIG. 1 shows an embodiment that may be particularly desirable when FIFO memory 10 is implemented on an appropriately constructed programmable logic device. (An example of a programmable logic device suitable for use in implementing this and all other portions of FIFO memory 10 is shown in commonly assigned, concurrently filed U.S. patent application No. 09/761,602 ~~(Docket No. 174/189)~~, now U.S. Patent No. 6,411,124, which is hereby incorporated by reference herein in its entirety. Programmable logic device implementation of FIFO memory 10 is further discussed later in this specification.) In the embodiment shown in FIG. 1 four logic modules 22 on the programmable logic device are programmed to count successive WCLK signal pulses and to produce a Gray code output 24 indicative of the count. In particular, each of logic modules 22 produces a respective one of the four-bits of the successive Gray code output words.

Please replace the paragraph starting on page 16, line 28, and ending on page 17, line 17, with the following amended paragraph:

If the invention is being implemented in a programmable logic device, it can be particularly helpful to use programmable logic device circuitry of the type shown in above-mentioned application No. 09/761,602 ~~(Docket No. 174/189)~~, now U.S. Patent No. 6,411,124. This is so because that reference shows programmable logic device logic modules that can perform all the functions performed by subcircuits 42 herein. In particular, all the functions performed by one subcircuit 42 herein can be performed in one logic module in the last-mentioned reference. In addition, the last- mentioned reference includes clock signal handling capabilities associated with each group or block of logic modules that facilitate including all the circuitry in FIG. 4 in one block of logic modules. One logic module in the block can receive a normal clock signal (like that needed by the right-most subcircuit 42 in FIG. 4) while other logic modules receive an inverted version of that same clock signal. The circuitry shown in the last-mentioned reference also facilitates stringing together the shift register capabilities of logic modules so that if shift registers longer than those employed in the examples described herein are needed, such longer shift registers can be readily provided.

Please replace the paragraph on page 21, lines 3-17, with the following amended paragraph:

Once again, if the invention is being implemented in a programmable logic device, it can be particularly helpful to use programmable logic device circuitry of the type shown in above-mentioned application No. 09/761,602 ~~(Docket No. 174/189))~~, now U.S. Patent No. 6,411,124, because (as has been mentioned) that circuitry includes logic modules that can readily perform all the functions required of subcircuits 62 herein. In particular, each subcircuit 62 can be implemented in one logic module in the last-mentioned reference. In addition, the last-mentioned reference shows circuitry that facilitates stringing together the shift register capabilities of logic modules if longer shift registers are needed to provide deeper FIFO memories (i.e., FIFO memories with capacity for more data words).